IN THE SPECIFICATION:

Please add the following new paragraphs on page 5, between lines 11 and 12 (immediately below the heading "Disclosure of the Invention"):

According to a first aspect of the present invention, there is provided a digital pulse width modulation generator for pulse width modulating a digital input signal comprising a single data bit and a sign bit, comprising:

an up/down digital counter (46), the up/down input counter (46) being controlled by the sign bit of the digital input signal;

an AND gate (45) having a first input which is clocked continuously by a first clock signal, a second input which receives the data bit of the digital input signal, and an output connected to the clock input of the up/down counter (46);

a second digital counter (42) clocked continuously by a constant rate, second clock signal;

a digital magnitude comparator (43) which compares the outputs of the two counters (42, 46) so that the greater-than or less-than output of the magnitude comparator (43) provides a pulse width modulation output signal, whereby the value represented by the pulse width modulation output signal is a ramp when the data bit of the digital input signal is at logic one and is a static value when the data bit of the digital input signal is at logic zero, the slope of the ramp being determined by the polarity of the sign bit of the digital input signal.

Please amend the paragraph starting on page 5, lines 12 through 15 as follows:

According to a ~~first~~ second aspect of the present invention, there is provided a digital pulse-width modulation generator for pulse width modulating a digital input signal comprising a single data bit and a sign bit, comprising: